MOSFET Switching Loss Model and Optimal Design of a Current Source Driver Considering the Current Diversion Problem

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***Abstract*—A new analytical switching loss model for power MOSFETs driven by the current source driver (CSD) is presented in this paper. The gate current diversion problem, which commonly exists in existing CSDs, is analyzed mathematically. In addition, a new accurate switching loss model considering every switching interval piecewisely is proposed. Based on the proposed loss model, the optimal design of the CSD inductor is achieved to minimize the total power loss for the buck converter. The experimental result verifies the proposed switching loss model and optimal design. The measured loss matches the calculated loss very well; the error between the calculated loss and measured one is less than 10% from 5 A load to 30 A load with 12 V input and 1.3 V output. As compared with the previous study, the efficiency with the optimal CSD inductor is improved from 86.1% to 87.6% at 12 V input and 1.3 V/20 A output and from 82.4% to 84.0% at 12 V input and 1.3 V/30 A output at 1 MHz switching frequency. As compared with the commercial driver-MOSFETs from Renesas and International Rectifier, the buck converter with the optimal CSD still shows better performance.**

***Index Terms*—Buck converter, common source inductor, current source driver (CSD), current diversion problem, driver-MOSFET (DrMos), loss model, optimal design, power MOSFET, voltage regulator (VR).**

I. Introduction

As predicted by Moore's Law, the number of transistors on a chip will double about every two years, which has been verified by Intel in the past 40 years [1]. With more and more transistors on a microprocessor, power density has become a more critical parameter to evaluate the performance of voltage regulators (VRs) of a microprocessor.

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Recently, a great deal of effort has been made to increase the power density of the VRs. One interesting area is to replace the magnetic-based converter with switched capacitor (also called charge pump) that consists of the inductorless configuration [2]. However, the large current spike, high electromagnetic interference noise, and narrow range of the voltage regulation limit the application of the switched capacitor [3]–[5].

Another interesting research field, which especially attracts the attention of semiconductor industries, is to integrate the VR into a single integrated chip, or called system-on-a-chip (SoC) [6]–[8]. However, due to the tight cost requirement of the commercial products, the integration of the inductor with high-current handling capability becomes the bottleneck, limiting the present current level of the SoC under 12 A [9].

One of the practical ways is increasing the switching frequency of the VRs into megahertz range to improve the dynamic performance and reduce the size of the passive components [10]–[12]. As the frequency increases, the frequency-dependent losses such as switching loss and gate drive loss become a penalty for VRs driven with conventional voltage source drivers (VSDs) [13]–[15]. In order to recover the gate driver loss dissipated in the charge and discharge path in the conventional VSD, resonant gate drive (RGD) techniques are proposed [16]–[19]. However, while RGD can recover the gate energy loss—it cannot reduce the switching loss that is much higher than the gate loss in high-frequency applications.

Recently, current source drivers (CSDs) are proposed to reduce the switching loss by charging and discharging the MOSFET with a nearly constant current [20]–[23]. Another advantage of the CSDs is that the gate drive voltage of CSDs is bipolar [25], which means that CSDs can turn off the power MOSFET with a negative voltage. The CSD proposed in [21]–[23] can turn off the power MOSFET with -0.7 V, while the CSD presented in [24] and [26] can turn off the power MOSFET with -3.5 V. In comparison, conventional VSD can only turn off the power MOSFET with $+0.5$ V. Therefore, compared to VSD, CSDs can significantly reduce the turn-off loss that is the dominant part of the whole switching loss.

However, during the switching transitions, the current in the CS inductor is diverted, which reduces the effective driver current of the MOSFET. This is known as the current diversion problem that commonly exists in CSDs. Therefore, the current diversion problem needs to be analyzed mathematically in order to predict and optimize the performance of the CSDs more accurately.

An analytical loss model, which thoroughly analyzes the impact of the parasitic inductance in CSDs, is presented in [27] to evaluate the performance of the CSDs. In addition, a generalized method to optimize the overall performance of the buck converter with a CSD is analyzed in the proposed model. A piecewise model that enables quick calculation and estimation of the switching loss is also proposed in [28]. However, the current diversion problem, which reduces the effective gate current and the switching speed, has not been investigated yet.

In this paper, a new analytical switching loss model considering the current diversion problem is proposed; the effective gate charging and discharging current is accurately determined. Moreover, the optimal CS inductor is obtained to maximize the overall efficiency of the buck converter. Since the model focuses on the performance of the CSD during turn-on and turn-off transitions of control FET, the parasitic inductances such as common source inductance and switching loop inductance for control FET that affect the switching transition have been considered. There are also some other parasitic elements from the printed circuit board (PCB) such as on-board inductance between the control FET and synchronous rectifier (sync FET). However, pervious studies in [29] and [30] have demonstrated that the on-board inductance mainly affects the ringing performance of the converter, but would barely introduce additional loss. The on-board resistance result from the layout increases the absolute value of the overall loss; but it will not interfere with the optimization procedure for the CSD as the performance of the CSD is independent of the parasitic resistance.

The proposed switching loss model is presented in Section II of this paper. Section III explains the procedures to obtain the optimal CS inductor. The experimental results of a synchronous buck converter with 12 V input, 1.2 V/30 A output, 1 MHz switching frequency, and discussions are presented in Section IV to validate the proposed loss model and optimal design of the CSD. Finally, the conclusions are drawn in Section V.

II. Proposed Switching Loss Model Considering the Current Diversion

This section presents the operation principles of the CSD and a new switching loss model considering the gate current diversion problem.

The equivalent circuit of the MOSFET driven by the proposed CSD is shown in Fig. 1, where the power MOSFET Q is represented by a typical capacitance model, L_S is the common source inductance including the PCB track and the bonding wire inside the MOSFET package, and L_D is the switching loop inductance.

For the purpose of the transient analysis, the following assumptions are made [31]:

1) when $v_{\rm CGS} < V_{\rm TH}$, MOSET is OFF and $I_{\rm DS} = 0$ ($t < t_1$ or $t > t_4$ in Fig. 2);
2) when $v_{\rm CGS} > V_{\rm TH}$ and $v_{\rm DS} > i_{\rm DS} R_{\rm DS(ON)}$, MOSFET is active and $i_{\rm DS} = g_{\rm FS}\,(v_{\rm CGS} - V_{\rm TH})$ ($t_1 < t < t_2$ or $t_3 < t < t_4$ in Fig. 2); and

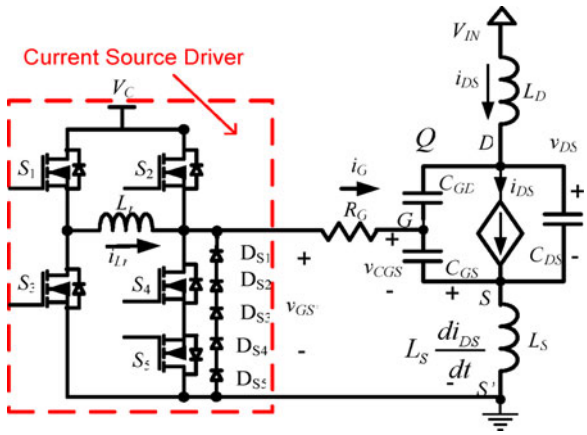

Fig. 1. Equivalent circuit of MOSFET with the proposed CSD.

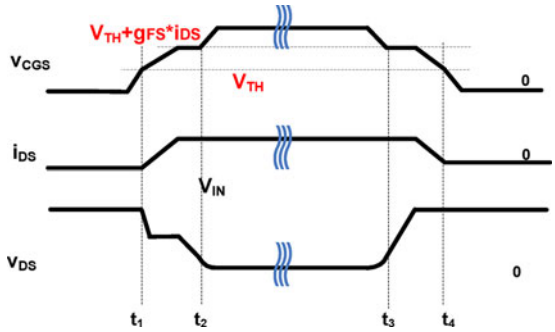

Fig. 2. Assumptions for power MOSFET for transient analysis.

3) when $g_{\rm FS}\,(v_{\rm CGS} - V_{\rm TH}) > v_{\rm DS}/R_{\rm DS(ON)}$, the MOSFET is fully ON ($t_2 < t < t_3$ in Fig. 2);

where $i_{\rm DS}$ is the drain current of the Q, $g_{\rm FS}$ is the transconductance, $v_{\rm DS}$ is the voltage across the drain–source capacitance of the Q, $v_{\rm CGS}$ is the voltage across the gate–source capacitance of the Q, $V_{\rm TH}$ is the threshold voltage of Q, $R_{\rm DS(ON)}$ is the ON-state resistance of Q.

During the *active state* when switching loss happens

$$i_{\rm DS} = g_{\rm FS}(v_{\rm CGS} - V_{\rm TH}). \tag{1}$$

According to Fig. 1, i_G is the effective current to charge or discharge Q as shown in

$$i_G = (C_{\rm GS} + C_{\rm GD})\frac{dv_{\rm GS}}{dt} - C_{\rm GD}\frac{dv_{\rm DS}}{dt} \tag{2}$$

and $v_{\rm DS}$ is given as

$$v_{\rm DS} = V_{\rm IN} - L_D\frac{di_{\rm DS}}{dt} - L_S\frac{d(i_{\rm DS} + i_G)}{dt}. \tag{3}$$

The detailed switching waveforms are illustrated in Fig. 3, where $v_{\rm GS1}$ to $v_{\rm GS5}$ are the gate drive signals for driver switches S_1 to S_5 in Fig. 1, i_{Lr} is the driver inductor current of L_r; $v_{\rm GS'}$, as shown in (4), is the gate–source voltage of Q including the effect of the common source inductance and the gate resistance, and $P_{\rm SW}$ is the switching loss of the Q

$$v_{\rm GS'} = -i_G R_G + v_{\rm CGS} - L_S\frac{d}{dt}(i_{\rm DS} + i_G). \tag{4}$$

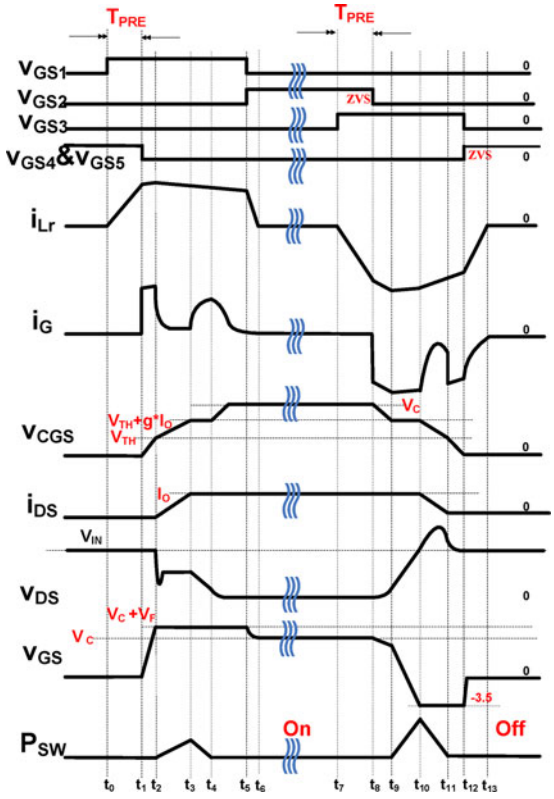

Fig. 3. MOSFET switching transition waveforms.

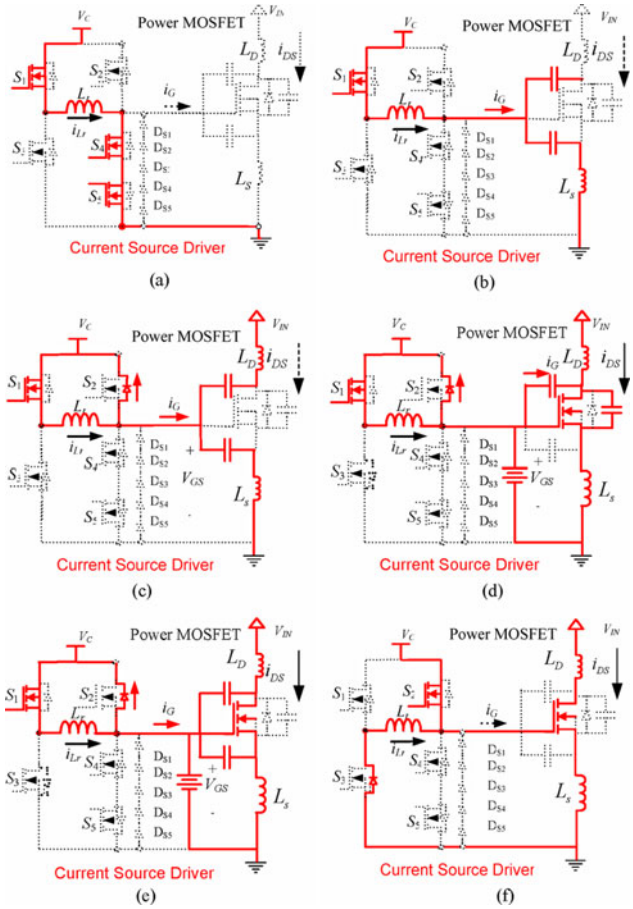

Fig. 4. Turn-on transition. (a) (t_0, t_1): precharge. (b) (t_1, t_2): turn-on delay. (c) (t_2, t_3): drain current rising. (d) (t_3, t_4): Miller plateau. (e) (t_4, t_5): remaining gate charging. (f) (t_5, t_6): energy recovery.

The operation principle of the turn-on transition is presented as follows. Prior to t_0, the power MOSFET is clamped in the OFF state by S_4 and S_5. It is noted that it is difficult to derive accurate equations for the MOSFET capacitances due to their nonlinear characteristic and limited information from the datasheet as well. So, in this paper, the capacitances of MOSFET have been assumed to be constant as approximation, despite that some errors might be introduced.

A. Turn-on Transition

Precharge [t_0, t_1]: At t_0, S_1 is turned on and the inductor current i_{Lr} rises almost linearly and the interval ends at t_1 that is preset by the designer. The equivalent circuit is given in Fig. 4(a). The inductor current i_{Lr} is given in (5). The duration of this interval equals $T_{\rm PRE}$

$$i_{Lr} \approx \frac{V_C(t-t_0)}{L_r}. \tag{5}$$

Turn-on Delay [t_1, t_2]: At t_1, S_4 and S_5 are turned off; the inductor current i_{Lr} starts to charge the gate capacitance of Q—the equivalent circuit is given in Fig. 4(b). At this interval, the effective charge current i_G equals i_{Lr}. The initial condition of this interval is $i_{Lr\_t1} = i_{Lr}(t_1 - t_0)$ and $v_{\rm CGS\_t1} = 0$. This interval ends when $v_{\rm CGS}$ reaches $V_{\rm TH}$. The differential equations for the circuit are given in (6), where $R_{\rm ON} = R_{\rm DSON\_S2} + R_{Lr} + R_G$, $R_{\rm DSON\_S2}$ is the on-resistance of S_2, R_{Lr} is the dc resistance (DCR) of L_r, and R_G is the gate resistance of the power MOSFET

$$V_C = (L_r + L_S)\frac{d}{dt}(i_{Lr}) + i_{Lr}R_{\rm ON} + v_{\rm CGS}$$
$$i_{Lr} = (C_{\rm GS} + C_{\rm GD})\frac{d}{dt}(v_{\rm CGS}). \tag{6}$$

Mathematically, there are three possible forms for the equation of the inductor current: over damped, critically damped, and under damped—for practical situations, $\omega_0 > \alpha_0$, the equations for i_G, i_{Lr}, and $v_{\rm CGS}$ are in the format of under damped as given in

$$v_{\rm CGS} = \left[A_0 \cos\left(\sqrt{\omega_0^2 - \alpha_0^2}t\right) + B_0 \sin\left(\sqrt{\omega_0^2 - \alpha_0^2}t\right)\right]e^{-\alpha_0 t} + C_0 \tag{7}$$

$$i_G = i_{Lr} = (C_{\rm GS} + C_{\rm GD})\left[\left(-A_{01}\sqrt{\omega_0^2 - \alpha_0^2} + B_0\alpha_0\right) \times \sin\left(\sqrt{\omega_0^2 - \alpha_0^2}t\right) + \left(-A_0\alpha - B_0\sqrt{\omega_0^2 - \alpha_0^2}\right) \times \cos\left(\sqrt{\omega_0^2 - \alpha_0^2}t\right)\right]e^{-\alpha_0 t} \tag{8}$$

where

$$\alpha_0 = \frac{R_{\rm ON}}{2(L_r + L_S)}$$

$$\omega_0 = \frac{1}{\sqrt{(L_r + L_S)\,(C_{\rm GS} + C_{\rm GD})}}$$

$$A_0 = \frac{-[2\alpha_0 i_{Lr\_t1} + (V_C - 2i_{Lr\_t1}R_{\rm ON})/(L_r + L_S)]}{[(C_{\rm GS} + C_{\rm GD})\,\omega_0^2]}$$

$$B_0 = \frac{i_{Lr\_t1} + (C_{\rm GS} + C_{\rm GD})\,\alpha_0 A_0}{[(C_{\rm GS} + C_{\rm GD})\,\omega_0^2]} \quad \text{and} \quad C_0 = -A_0$$

Drain Current Rising [t_2, t_3]: At t_2, $v_{\rm CGS} = V_{\rm TH}$. During this interval, $v_{\rm CGS}$ keeps increasing and $i_{\rm DS}$ starts to rise according to the relationship in (1). Since $i_{\rm DS}$ flows through L_S, according to (4), the voltage induced across L_S makes $v_{\rm GS'}$ larger than the driver supply voltage V_C. Therefore, D_2, the body diode of the driver switch S_2, is driven on to clamp $v_{\rm GS'}$ at $V_C + V_F$, where V_F is the forward voltage of D_2.The equivalent circuit is shown in Fig. 4(c). At this interval, i_G drops sharply because of the voltage clamping. The subtraction of i_{Lr} and i_G is diverted into D_2. The initial condition of this interval is $i_{G\_t2} = i_G(t_2 - t_1)$, $i_{\rm DS\_t2} = 0$, and $v_{\rm CGS\_t2} = V_{\rm TH}$. The interval ends at t_3 when $i_{\rm DS}$ equals the load current I_O.

Mathematically, there are three possible forms for the equation of the inductor current—for practical situations, $\omega_1 < \alpha_1$, the equations for i_G, i_{Lr}, and $v_{\rm CGS}$ are in the format of over damped as given in (9)–(13). It is noted that from (13), i_G is largely determined by L_S: the larger L_S is, the smaller i_G is

$$v_{\rm CGS} = A_1 e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2})t} + B_1 e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2})t} + C_1 \quad (9)$$

$$i_{\rm DS} = g_{\rm FS}(v_{\rm CGS} - V_{\rm TH}) = g_{\rm FS}(A_1 e^{\left(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}\right)t} + B_1 e^{\left(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}\right)t} + C_1 - V_{\rm TH}) \quad (10)$$

$$i_G = A_1\left(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}\right) e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2})t} + B_1\left(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}\right) e^{\left(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}\right)t} \quad (11)$$

$$i_{Lr} = \left(I_{G\_t2} + \frac{V_F}{R_G}\right) e^{(-R_G/L_r)t} - \frac{V_F}{R_G} \quad (12)$$

$$v_{\rm DS} = V_{\rm IN} - L_D\frac{d}{dt}(i_G) - (L_S + L_D)\frac{d}{dt}(i_{\rm DS}) \quad (13)$$

were

$$\omega_1 = 1\sqrt{L_S\,(C_{\rm GS} + C_{\rm GD})}$$

$$\alpha_1 = \frac{[R_G\,(C_{\rm GS} + C_{\rm GD}) + L_S g_{\rm FS}]}{[L_S\,(C_{\rm GS} + C_{\rm GD})]}$$

$$C_1 = V_F + V_c$$

$$A_1 = \frac{\left[(V_{\rm TH} - V_F - V_C)\left(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}\right) - I_{G\_t2}\right]}{\left[2\sqrt{\alpha_1^2 - \omega_1^2}\right]},$$

$$\text{and} \quad B_1 = V_{\rm TH} - A_1 - C_1$$

Miller Plateau [t_3, t_4]: At t_3, $i_{\rm DS} = I_O$. During this interval, $v_{\rm CGS}$ is held at the Miller plateau voltage, and i_G mainly flows through the gate-to-drain capacitance of Q and $v_{\rm DS}$ decreases accordingly. It is noted that i_G starts to rapid increase since the electromotive force (EMF) across L_s falls sharply due to the unchanged $i_{\rm DS}$; however, part of the inductor current is still diverted through D_2. The equivalent circuit is given in Fig. 4(d). The initial values of the interval are $i_{G\_t3} = i_G(t_3 - t_2)$, $v_{\rm CGS\_t3} = v_{\rm CGS}(t_3 - t_2)$, and $v_{\rm DS\_t3} = v_{\rm DS}(t_3 - t_2)$. The interval ends when $v_{\rm DS}$ equals to zero at t_4. The equations for i_G, $v_{\rm CGS}$, and $v_{\rm DS}$ are given in (14) and (15) and i_{Lr} remains the same as the previous interval

$$v_{\rm CGS} = V_{\rm CGS\_t3} \quad (14)$$

$$i_G = \left[I_{G\_t3} - \frac{(V_C + V_F - V_{\rm CGS\_t3})}{R_G}\right] e^{(-R_G/L_s)t} + \frac{(V_C + V_F - V_{\rm CGS\_t3})}{R_G} \quad (15)$$

$$v_{\rm DS} = \left(\frac{I_{G\_t3} - (V_C + V_F - V_{\rm CGS\_t3})/R_G}{C_{\rm GD}R_G/L_s}\right) e^{(-R_G/L_s)t} - \frac{(I_{G\_t3} - (V_C + V_F - V_{\rm CGS\_t3})/R_G)t}{C_{\rm GD}} + \left(V_{\rm DS\_t3} - \frac{I_{G\_t3} - (V_C + V_F - V_{\rm CGS\_t3})/R_G}{C_{\rm GD}R_G/L_s}\right). \quad (16)$$

Remaining Gate Charging [t_4, t_5]: At t_4, $v_{\rm DS} = 0$ and $v_{\rm CGS}$ starts to rise again until it reaches V_C; $v_{\rm GS'}$ remains at $V_C + V_F$, and due to the rising of the $v_{\rm CGS}$, i_G decreases gradually. The equivalent circuit is given in Fig. 4(e). The initial values of this interval are: $i_{G\_t4} = i_G(t_4 - t_3)$, $v_{\rm CGS\_t4} = v_{\rm CGS\_t3}$, and $v_{\rm DS\_t4} = v_{\rm DS}(t_4 - t_3)$. This interval ends at t_5 when $v_{\rm CGS} = V_C$.

Mathematically, there are three possible forms for the equation of the inductor current—for practical situations, $\omega_2 < \alpha_2$; therefore, equations for i_G, $v_{\rm CGS}$, and $v_{\rm DS}$ are in the format of over damped given in ((16))–((19)) and i_{Lr} is the same as the previous interval

$$v_{\rm CGS} = \left[A_2\,\cos\left(\sqrt{\alpha_2^2 - \omega_2^2}t\right) + B_2\,\sin\left(\sqrt{\alpha_2^2 - \omega_2^2}t\right)\right] e^{-\alpha_2 t} + C_2 \quad (17)$$

$$i_G = (C_{\rm GS} + C_{\rm GD})\left[\left(-A_2\sqrt{\alpha_2^2 - \omega_2^2} + B_2\alpha_2\right)\right.$$

$$\sin\left(\sqrt{\alpha_2^2-\omega_2^2}t\right)+\left(-A_2\alpha_2-B_2\sqrt{\alpha_2^2-\omega_2^2}\right)\cos\left(\sqrt{\alpha_2^2-\omega_2^2}t\right)\Big]e^{-\alpha_2 t} \tag{18}$$

$$v_{\rm DS}=V_{\rm DS\_t4}-\frac{(v_{\rm CGS}-V_{\rm DS\_t4})(V_{\rm DS\_t4}-I_O R_{\rm ON@V_c})}{V_C-V_{\rm CGS\_t4}} \tag{19}$$

where $\omega_2=1/\sqrt{L_S\,(C_{\rm GS}+C_{\rm GD})}, \alpha_2=R_G/L_S$, $A_2=V_{\rm CGS\_t3}-C_2, B_2=[I_{G\_t4}/(C_{\rm GS}+C_{\rm GD})-A_2\alpha_2]/\sqrt{\alpha_2^2-\omega_2^2}$, $C_2=V_C+V_F$, and $R_{\rm ON@VC}$ is the on-resistance of the MOSFET when $V_{\rm CGS}=V_C$

Energy Recovery [t_5, t_6]: At t_5, S_2 is turned on to recover the energy stored in the inductor to the source as well as actively clamping Q to V_C. The initial value of this interval is $i_{Lr\_t5}=i_{Lr}(t_5-t_2)$, and this interval ends when i_{Lr} becomes zero. The equivalent circuit is illustrated in Fig. 4(f). The equation for i_{Lr} is in (20). It is noted that the current slew rate of this interval is larger than that of the *precharge* interval due to the larger voltage drop across the inductor L_r during this interval

$$i_{Lr}=\left[I_{G\_t5}+\frac{(V_C+V_F)}{(R_{\rm ON\_S2}+R_{L_r})}\right]e^{[-(R_{\rm ON\_S2}+R_{Lr})/L_r]t}-\frac{(V_C+V_F)}{(R_{\rm ON\_S2}+R_{L_r})}. \tag{20}$$

B. Turn-off Transition

In this section, the turn-off transition is analyzed. Prior to t_7, the power MOSFET is clamped in the ON state by S_2.

Predischarge [t_7, t_8]: At t_7, S_3 is turned on and the inductor current i_{Lr} rises almost linearly and the interval ends at t_8 that is preset by the designer. The equivalent circuit is shown in Fig. 5(a). The equation for i_{Lr} is given in (21). The duration of this interval equals $T_{\rm PRE}$

$$i_{Lr}\approx-\frac{V_C(t-t_7)}{L_r}. \tag{21}$$

Turn-off Delay [t_8, t_9]: At t_8, S_2 is turned off. In this interval, $v_{\rm CGS}$ decreases until $V_{\rm TH}+I_{O\times}g_{\rm FS}$ that ends the interval. The equivalent circuit is given in Fig. 5(b). The initial condition of this interval is $i_{G\_t8}=i_{Lr\_t8}=i_{Lr}$ (t_8) and $v_{\rm CGS\_t8}=V_C$. The way to solve the equations for i_G, i_{Lr}, and $v_{\rm CGS}$ is the same as *turn*-on *delay* interval.

Miller Plateau [t_9, t_{10}]: At t_9, $v_{\rm CGS}=V_{\rm TH}+I_{O\times}g_{\rm FS}$. In this interval, $v_{\rm CGS}$ holds at the Miller plateau voltage, $V_{\rm TH}+I_{\rm O}\times g_{\rm FS}$. i_G (equal to i_{Lr}) strictly discharges the gate-to-drain capacitance $C_{\rm GD}$ of Q and $v_{\rm DS}$ rises until it reaches $V_{\rm IN}$ at t_{10}. The equivalent circuit is illustrated in Fig. 5(c). The equations of this interval can be obtained in the same way as the *Miller plateau* in turn-on interval.

Drain Current Drop [t_{10}, t_{11}]: At t_{10}, $v_{\rm DS}=V_{\rm IN}$ and $v_{\rm CGS}$ continues to decrease from $V_{\rm TH}+I_{\rm O}\times g_{\rm FS}$ to $V_{\rm TH}$. $i_{\rm DS}$ falls from I_O to zero according to relationship in (1). According to (4), due to the induction EMF across L_s, the series-connected diodes D_{S1} to D_{S5} are driven on to clamp $v_{\rm GS'}$ at around -3.5 V.

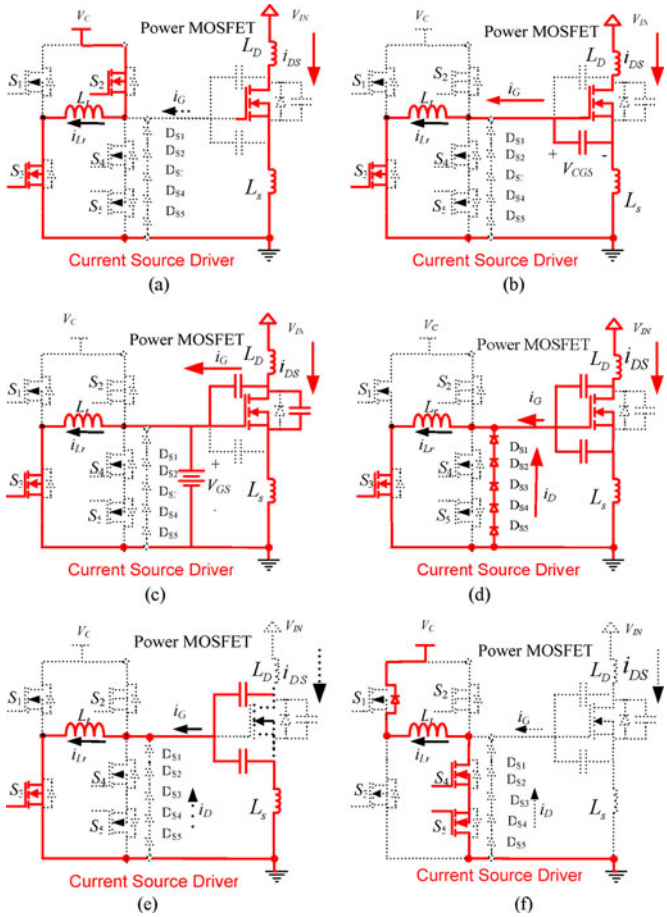

Fig. 5. Turn-off transition. (a) (t_7, t_8): predischarge. (b) (t_8, t_9): turn-off delay. (c) (t_9, t_{10}): Miller plateau. (d) (t_{10}, t_{11}): drain current drop. (e) (t_{11}, t_{12}): remaining gate discharge. (f) (t_{12}, t_{13}): energy recovery.

The voltage across the CS inductor becomes -3.5 V, so i_{Lr} decreases at a higher rate than in the turn-on transition. The equivalent circuit of this interval is given in Fig. 5(d).

By comparison, the CSD proposed in [21] can only clamp $v'_{\rm GS}$ to -0.7 V during this interval. According to [25], the CSD in [21] turns off the power MOSFET within 15.6 ns, while the turn-off time of the CSD shown in this paper is 8.7 ns. This means that the turn-off loss of the CSD in this paper (see Fig. 1) is much smaller than that of the CSD in [21]. It is worth mentioning that $v_{\rm DS}$ in this interval will keep rising due to effect of the L_S. Therefore, the derivation of the equations in this interval needs to solve the third-order differential equations set in

$$\begin{cases} L_S\dfrac{d}{dt}(i_{\rm DS}+i_G)+v_{\rm CGS}+i_G R_{\rm G}+V_{\rm F}=0 \\ i_{\rm DS}=g_{\rm FS}(v_{\rm CGS}-V_{\rm TH}) \\ i_G=(C_{\rm GS}+C_{\rm GD})\dfrac{d}{dt}(v_{\rm CGS})-C_{\rm GD}\dfrac{d}{dt}(v_{\rm DS}) \\ L_S\dfrac{d}{dt}(i_G)+(L_D+L_S)\dfrac{d}{dt}(i_{\rm DS})+v_{\rm DS}-V_{\rm IN}-V_F=0. \end{cases} \tag{22}$$

Remaining Gate Discharging [t_{11}, t_{12}]: At t_{11}, $v_{\rm CGS}=V_{\rm TH}$. In this interval, $v_{\rm CGS}$ continues to decrease until it equals zero; it is noted that $v_{\rm DS}$ continues to rise during this interval. The equivalent circuit is shown in Fig. 5(e). The equations in this

interval have the same form as the equations in *remaining gate charging* interval.

Energy Recovery [t_{12}, t_{13}]: At t_{12}, S_4 and S_5 are turned on to recover the energy stored in the inductor to the source as well as actively clamping Q to ground. The equivalent circuit is given in Fig. 5(f). This interval is the same as the *energy recovery* in turn-on transition.

C. Total Loss for the Power MOSFET Driven With the Proposed CSD

In this section, the procedure to calculate the total loss of the power MOSFET driven with the proposed CSD will be explained.

1) Turn-on loss $P_{\mathrm{SW\_ON}}$ equals the energy lost in each turn-on transition times F_S, where F_S is the switching frequency. As expressed in (23), before turn-on transition begins, some energy has already been stored in the output capacitance of the MOSFET. This energy together with the energy supplied by the source is dissipated through the turn-ON transition

$$P_{\mathrm{SW\_ON}} = E_{\mathrm{Lost\_ON}} \times F_S = \left(\frac{C_{\mathrm{oss}} \times Q_{\mathrm{oss}}}{2} + \int_{t2}^{t4} (i_{\mathrm{DS}} \times v_{\mathrm{DS}}) dt \right) \times F_S. \tag{23}$$

Turn-off loss $P_{\mathrm{SW\_OFF}}$ equals the energy lost in each turn-off transition times F_S. After turn-off transition ends, some energy is still stored in the output capacitance of the MOSFET; therefore, $P_{\mathrm{SW\_OFF}}$ can be derived in

$$P_{\mathrm{SW\_OFF}} = E_{\mathrm{Lost\_OFF}} \times F_S = \left(\int_{t9}^{t11} (i_{\mathrm{DS}} \times v_{\mathrm{DS}} \times F_S) dt - \frac{C_{\mathrm{oss}} \times Q_{\mathrm{oss}}}{2} \right) \times F_S. \tag{24}$$

Switching loss P_{SW} equals the sum of turn-on loss $P_{\mathrm{SW\_ON}}$ and turn-off loss $P_{\mathrm{SW\_OFF}}$ as derived in

$$P_{\mathrm{SW}} = P_{\mathrm{SW\_ON}} + P_{\mathrm{SW\_OFF}}. \tag{25}$$

2) The gate driver loss P_{DR} is made up of conduction loss $P_{\mathrm{DR\_COND}}$, gate drive loss $P_{\mathrm{DR\_GATE}}$, and output loss $P_{\mathrm{DR\_OUT}}$ as given in

$$P_{\mathrm{DR}} = P_{\mathrm{DR\_COND}} + P_{\mathrm{DR\_GATE}} + P_{\mathrm{DR\_OUT}}. \tag{26}$$

3) Conduction loss P_{COND} is calculated in (27), where I_O is the drain-to-source current when power MOSFET is ON, $R_{\mathrm{DS(ON)}}$ is the on-resistance of the MOSFET, T_{ON} is the ON time, and T_S is the switching cycle

$$P_{\mathrm{COND}} = I_O^2 \times R_{\mathrm{DS(ON)}} \times \frac{T_{\mathrm{ON}}}{T_S}. \tag{27}$$

4) The total loss for the power MOSFET driven with the proposed CSD, P_{SUM}, is

$$P_{\mathrm{SUM}} = P_{\mathrm{DR}} + P_{\mathrm{SW}} + P_{\mathrm{COND}}. \tag{28}$$

III. Optimal Design of Inductor Value of the CSD

According to [21], the rms current of the CS inductor L_r during the precharge and predischarge interval, I_{Lr_rms}, is calculated in (29), where T_{PRE} is the precharge time ($t_0 - t_1$) and predischarge time ($t_7 - t_8$). Therefore, the conduction loss at these two intervals is positively related to the precharge time T_{PRE}

$$I_{Lr\_\mathrm{rms}} \approx i_{Lr\_t1} \times \sqrt{\frac{T_{\mathrm{PRE}} \times F_S}{3}} \approx \frac{V_C \times T_{\mathrm{PRE}}}{L_r} \times \sqrt{\frac{T_{\mathrm{PRE}} \times F_S}{3}}. \tag{29}$$

As the current in the CS inductor between Fig. 4(b)–(e) and Fig. 5(b)–(e) roughly remains constant; therefore, the rms current for these two intervals is approximately the same as i_{Lr_t1}

The rms current during Figs. 4(f) and 5(f) is approximately the same as (29) according to [21]. Therefore, T_{PRE} should be set as short as possible within the practical limits of the driver to minimize the conduction loss. Taken the logic limits into consideration, T_{PRE} is set to be 20 ns, and it needs to be pointed out that the design procedure presented here is also applicable to other conditions.

In order to maximize the overall efficiency of the buck converter with the proposed CSD, P_{SUM} should be minimized. Since the conduction loss and output loss for power MOSFET are relatively constant for the given duty cycle and load current, the optimal design of the CSD involves a trade-off between driver loss and switching loss, and there is an optimal inductor current I_{Lr_OPT}, where P_{SUM} reaches the minimal value as illustrated in [27]. It is noted that it is hard to derive the equations of P_{SUM} with inductor current I_{Lr} as the only variable. Therefore, in this paper, the optimal inductor current where P_{SUM} becomes minimal is obtained in a numerical way—in other words, P_{SUM} are plotted versus different inductor current values I_{Lr}, from which the optimal inductor current I_{Lr_OPT} is approximately obtained. With T_{PRE} fixed to 20 ns and according to (29), it can be inferred that there is also an optimal CS inductor L_{r_OPT}, corresponding to the optimal inductor current I_{Lr_OPT}, as given in

$$L_{r\_\mathrm{OPT}} = \frac{V_C \times T_{\mathrm{PRE}}}{I_{Lr\_\mathrm{OPT}}}. \tag{30}$$

To validate the analysis, the following conditions are used: $V_{\mathrm{IN}} = 12\,\mathrm{V}$, $V_O = 1.3\,\mathrm{V}$, $I_O = 30\,\mathrm{A}$, $V_C = 5\,\mathrm{V}$, $F_S = 1\,\mathrm{MHz}$, *Q:* SI7386DP, drive switches S_1–S_4: FDN335, and antidiodes D_{S1}–D_{S5}: MBR0520. Typically, the parasitic inductance value for PowerPAK SO-8 package is tested by the semiconductor manufacturers in [32] and [33] and range from approximately 250 pH–1 nH. In this model, $L_S = 1$ nH and $L_D = 1$ nH are used. Fig. 6 illustrates the plot of the equation P_{SUM} versus the CSD inductor value within practical range by using MathCAD. It is noted that, in comparison with the driver loss, the switching loss is the dominant loss of the power MOSFET. It is observed that the optimal CS inductor is around 25 nH, where P_{SUM} is the minimum. As shown in Fig. 7, the peak inductor current at this moment equals 4A.

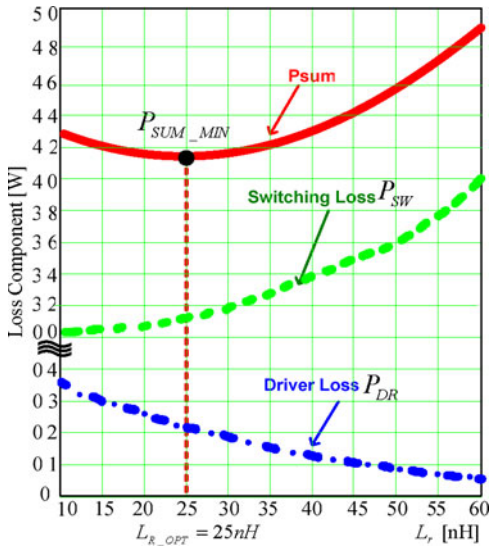

Fig. 6. Total loss versus CS inductor value.

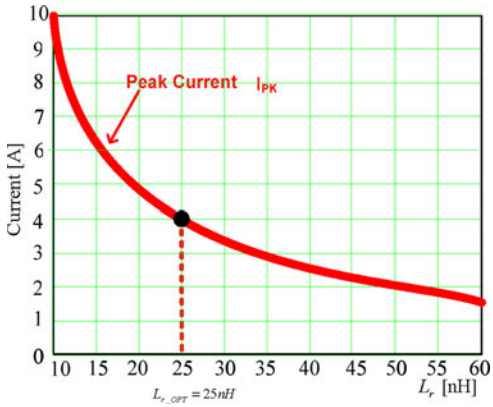

Fig. 7. Peak current versus CS inductor value.

IV. Experimental Results and Discussions

A. Hardware Setup

A prototype of a synchronous buck converter as shown in Fig. 8 was built to verify the proposed switching loss model and the optimal design of the CS inductor. The control FET of the converter is driven with the proposed CSD, while the sync FET is driven with a conventional VSD since the switching loss for sync FET is very small.

The PCB consists of six-layer, 4 oz copper, and the photograph of the prototype is shown in Fig. 9. The components used are: Q_1: Si7386DP; Q_2: IRF6691; output filter inductance: L_O = 330 nH (IHLP-5050CE-01); CS inductor: L_r = 23 nH (Coilcraft 2508-23 N_L); drive switches S_1–S_4: FDN335; and antidiodes D_{S1}–D_{S5}: MBR0520. Altera Max II EPM240 complex programmable logic device (CPLD) is used to generate the pulsewidth modulation signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. For common practice, the driver voltages for the control FET and sync FET are both set to be 5 V. The operating conditions

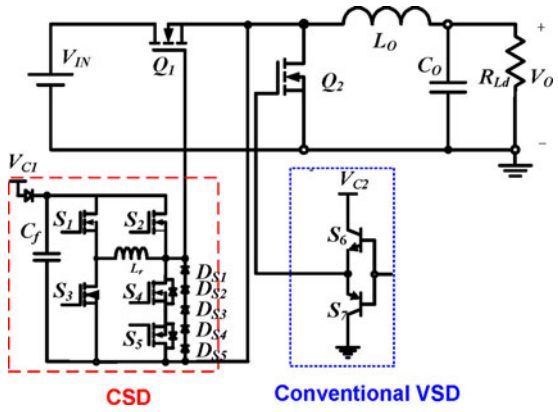

Fig. 8. Synchronous buck converter with the proposed CSD.

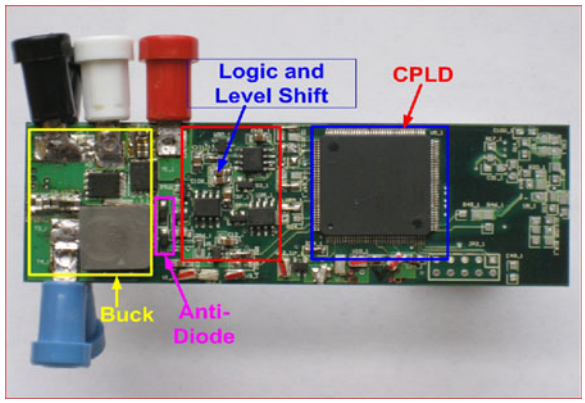

Fig. 9. Photograph of the buck converter driven with CSD shown in Fig. 1.

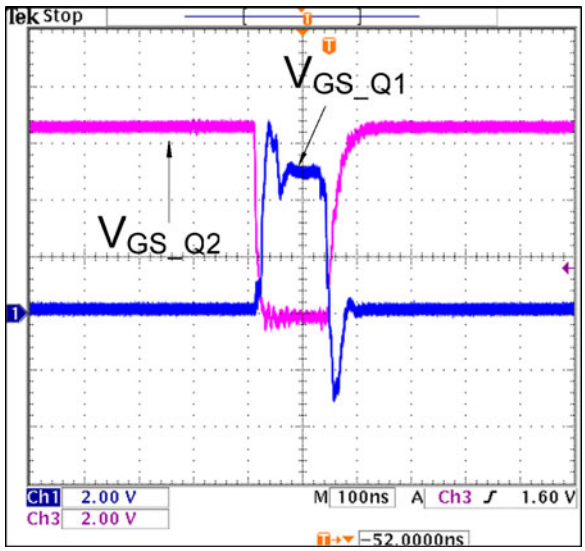

Fig. 10. Waveforms of driver signals V_{GS}_Q1 and V_{GS}_Q2.

are: input voltage V_{IN}: 12 V; output voltage V_O: 1.2–1.5 V; and switching frequency F_S: 500 kHz–1 MHz.

The gate driver signals for V_{GS_Q1} and V_{GS_Q2} are shown in Fig. 10. It is observed that during turn-off transition, V_{GS_Q1} is clamped to about −3.5 V. It is noted that V_{GS_Q1} is impacted the parasitic from the differential probe, so it is not exactly the

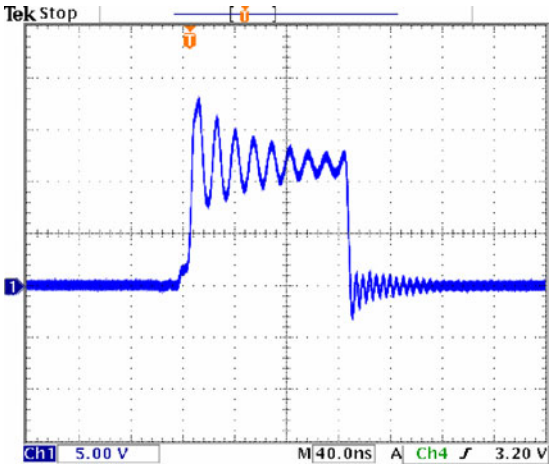

Fig. 11. Switching node waveform of the synchronous buck converter at 12 $V_{\rm IN}$, 1.2 $V_{\rm OUT}$, and 30 A.

same as the waveforms shown in Fig. 3. But it is clearly seen around about −3.5 V on $V_{{\rm GS}\_Q1}$. The current waveform of the CSD inductor is impossible to obtain without breaking the setup of the prototype, and therefore, is not provided.

It is noted that the breakdown voltage capability of control FET could be reduced due to the negative gate voltage $V_{{\rm GS}\_Q1}$. However, designers normally obey an 80% margin rule [34], which means that the maximum voltage stress measured across any MOSFET must not exceed 80% of the MOSFET's breakdown voltage. This requires both good layout design and reasonable selection of the MOSFET based on the application conditions [35]. The switching node waveform for synchronous buck converter at 12 $V_{\rm IN}$, 1.2 $V_{\rm OUT}$, and 30 A is shown in Fig. 11. It is observed that the voltage stress for sync FET is 18 V, while the voltage stress for control FET is 15 V; therefore, it still meets the requirements for the 80% margin in this design.

Figs. 12–14 illustrate the measured efficiencies comparison with 12 $V_{\rm IN}$/1.2 $V_{\rm OUT}$ at 500 kHz, 750 kHz and 1 MHz between the optimized bipolar CSD and VSD, which is implemented with Intersil synchronous buck gate driver ISL6613. It is observed that the optimized bipolar CSD has achieved better performance than the VSD at all conditions. The efficiency improvement achieved by the bipolar CSD at 30 A load is 1.4% at 500 kHz and 2.5% at 1 MHz. That is because the bipolar CSD, compared with VSD, achieves much lower the switching loss that is proportional to the switching frequency.

B. Verification and Discussions of the Proposed Switching Loss Model

1) Verification of the Proposed Switching Loss Model: In addition to the loss for control FET illustrated in Section II, the loss of the buck converter in Fig. 8 also includes the following major losses:

a) Loss for output inductor: Under continuous current mode, there is always current flowing through the output inductor. Therefore, the parasitic resistance of the output inductor, often called DCR, introduces conduction loss. The accurate calculation of this portion of loss should consider the ripple of the inductor current, as shown in Fig. 15.

Assuming that there is no iron loss in the inductor, the rms of the inductor current $I_{L\_{\rm rms}}$ is calculated in (31) [29]. And the conduction loss for inductor is calculated in (32), where I_O is the load current of the buck converter, V_O is the output voltage, $V_{\rm IN}$ is the input voltage, T_S is the switching cycle, L_O is the value of the output inductor, and DCR is the parasitic resistance of the output inductor

$$I_{L\_{\rm rms}} = \sqrt{\frac{\int_0^{DT_s} i_{\rm IN}^2 dt + \int_{DT_s}^{T_s} i_{\rm IN}^2 dt}{T_S}} \approx \sqrt{I_O^2 + \frac{I_O^2}{12}} \approx \sqrt{I_O^2 + \frac{V_O^2(V_{\rm IN} - V_O)^2 T_S^2}{12 L_O^2 V_{\rm IN}^2}} \tag{31}$$

$$P_L = I_{L\_{\rm rms}}^2 \times {\rm DCR} = \left[I_O^2 + \frac{V_O^2(V_{\rm IN} - V_O)^2 T_S^2}{12 L_O^2 V_{\rm IN}^2} \right] \times {\rm DCR} \tag{32}$$

b) Loss for sync FET of the buck converter: The loss for sync FET consists of conduction loss, gate driver loss, reverse recovery loss, and switching loss.

The energy supplied by the source to drive the sync FET is totally dissipated into heat during turn-on and turn-off transition. Therefore, the gate driver loss $P_{{\rm DR}\_{\rm SR}}$ is given in (33), where $Q_{G\_{\rm SR}}$ is the total gate charge for sync FET, $V_{C\_{\rm SR}}$ is the gate drive voltage for sync FET, and F_S is the switching frequency

$$P_{{\rm DR}\_{\rm SR}} = Q_{G\_{\rm SR}} \times V_{C\_{\rm SR}} \times F_S. \tag{33}$$

Conduction loss $P_{{\rm COND}\_{\rm SR}}$ is calculated in (34), where $I_{{\rm SR}\_{\rm rms}}$ is the rms current of the sync FET, $R_{{\rm DS(ON)}\_{\rm SR}}$ is the on-resistance of the sync FET, $T_{{\rm ON}\_{\rm SR}}$ is the ON time of the sync FET, $T_{\rm ON}$ is the ON time for Ctrl FET, and T_S is the switching cycle

$$P_{{\rm COND}\_{\rm SR}} = I_{{\rm SR}\_{\rm rms}}^2 \times R_{{\rm DS(ON)}\_{\rm SR}} \times \frac{T_S - T_{\rm ON}}{T_S}. \tag{34}$$

The body diode of sync FET contributes to reverse recovery loss due to the characteristic of p-i-n diode; also, the reverse recovery charge $Q_{{\rm RR}\_{\rm SR}}$ is highly dependent on the *di/dt* rate and forward current in the diode. In this paper, $Q_{{\rm RR}\_{\rm SR}}$ is obtained from datasheet for approximation. Reverse recovery loss for sync FET $P_{Q{\rm RR}\_{\rm SR}}$ is calculated in (35), where $V_{\rm IN}$ is the drain-to-source voltage across the sync FET when it is OFF

$$P_{Q{\rm RR}\_{\rm SR}} = V_{\rm IN} \times Q_{{\rm RR}\_{\rm SR}} \times F_S. \tag{35}$$

The output loss for sync FET $P_{{\rm OUT}\_{\rm SR}}$ is calculated in (36), where $Q_{{\rm OSS}\_{\rm SR}}$ is the charge for the output capacitance of the sync FET

$$P_{{\rm OUT}\_{\rm SR}} = \frac{V_{\rm IN} \times Q_{{\rm OSS}\_{\rm SR}} \times F_S}{2}. \tag{36}$$

The switching loss of the sync FET $P_{{\rm SW}\_{\rm SR}}$ is made up of the turn-on loss $P_{{\rm SW(ON)}\_{\rm SR}}$ and turn-off loss $P_{{\rm SW(OFF)}\_{\rm SR}}$

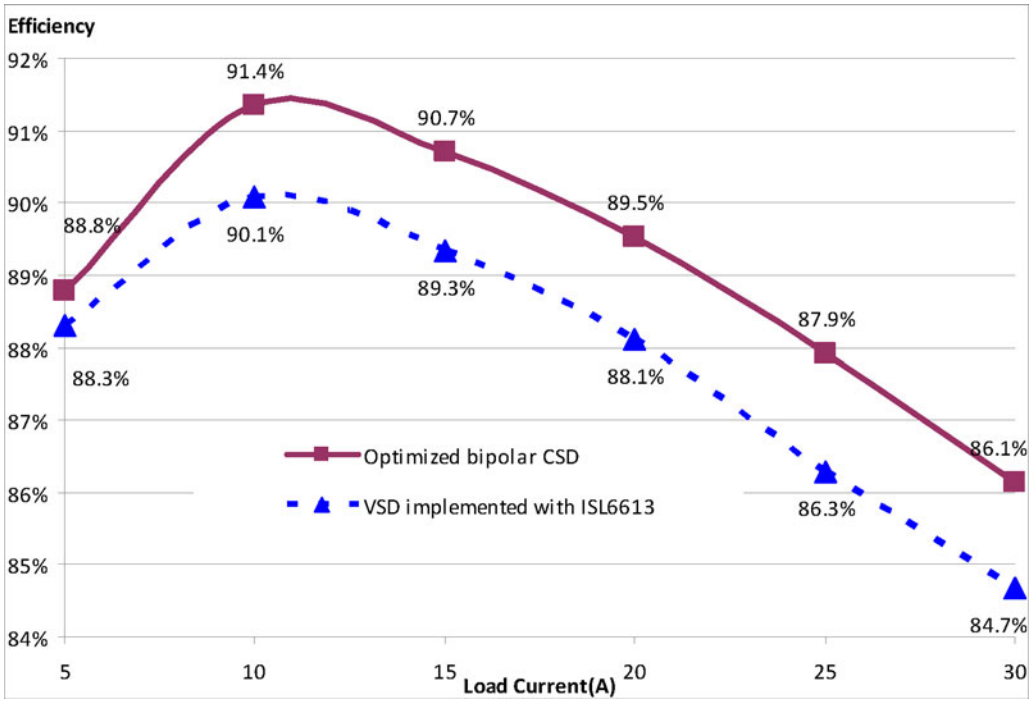

Fig. 12. Measured efficiency comparison between the bipolar CSD and VSD for 12 V_{IN} and 1.2 V_{OUT} at the frequency of 500 kHz.

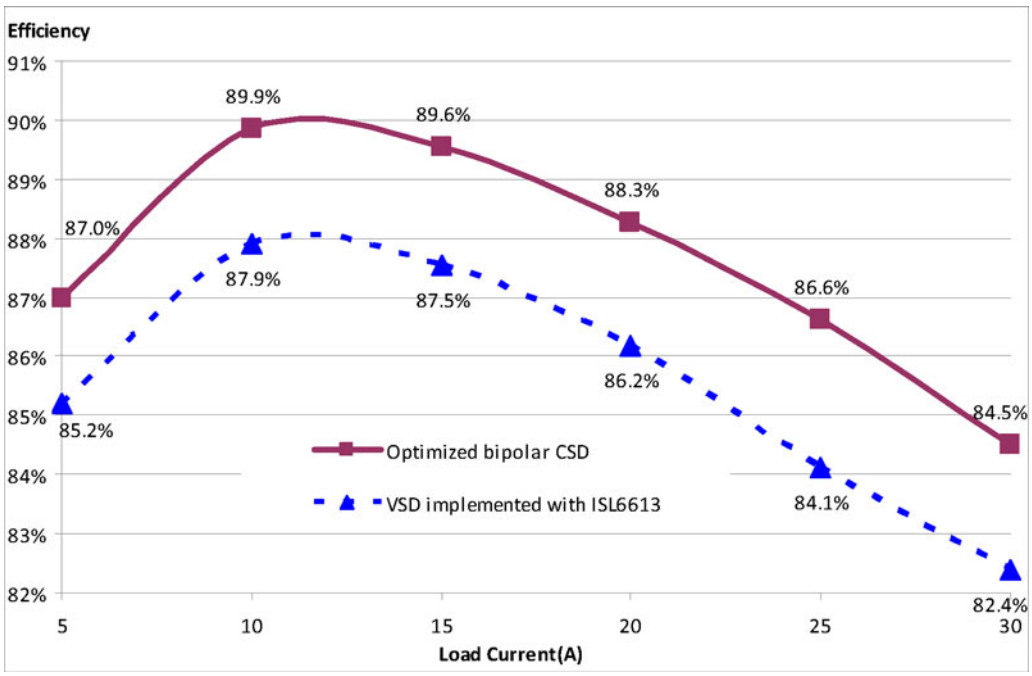

Fig. 13. Measured efficiency comparison between the bipolar CSD and VSD for 12 V_{IN} and 1.2 V_{OUT} at the frequency of 750 kHz.

of sync FET, as shown in

$$P_{\mathrm{SW\_SR}} = P_{\mathrm{SW(ON)\_SR}} + P_{\mathrm{SW(OFF)\_SR}}. \tag{37}$$

The turn-on loss and turn-off loss for sync FET equals the energy supplied by the source as there are no energy transfer on the output capacitance during turn-on and turn-off transitions. The equations for $P_{\mathrm{SW(ON)\_SR}}$ and $P_{\mathrm{SW(OFF)\_SR}}$ are shown in (38) and (39) proposed in [36], where $V_{\mathrm{TH\_SR}}$ is the gate threshold voltage of the sync FET, $g_{\mathrm{FS\_SR}}$ is the transconductance of the sync FET, $R_{\mathrm{DR\_SR}}$ is the on-resistance of the driver, $R_{G\text{-}\mathrm{SR}}$ is the gate resistance of the sync FET, $C_{\mathrm{ISS\_SR}}$ is the input capacitance of the sync FET, $V_{F\text{-}\mathrm{SR}}$ is the body diode forward voltage of sync FET, $V_{\mathrm{SPE\_SR}}$ is the specified gate voltage of the sync FET according to the datasheet, and $R_{\mathrm{DS(ON)\_SR}}$ is the on-resistance of the sync FET when gate drive voltage equals

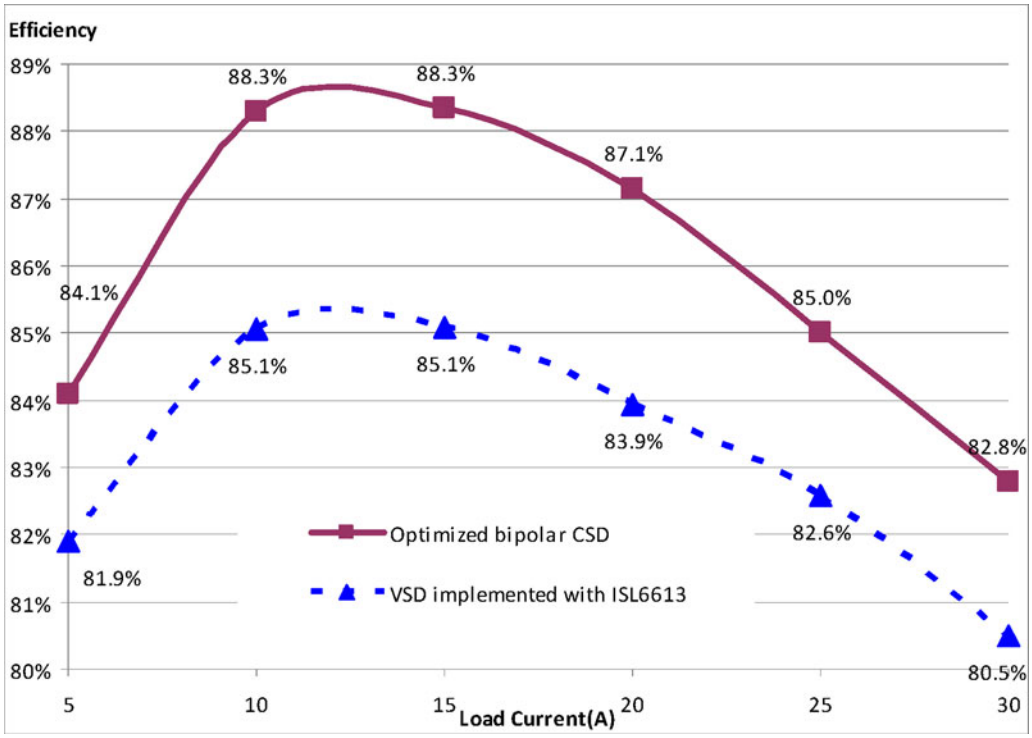

Fig. 14. Measured efficiency comparison between the bipolar CSD and VSD for 12 V_{IN} and 1.2 V_{OUT} at the frequency of 1 MHz.

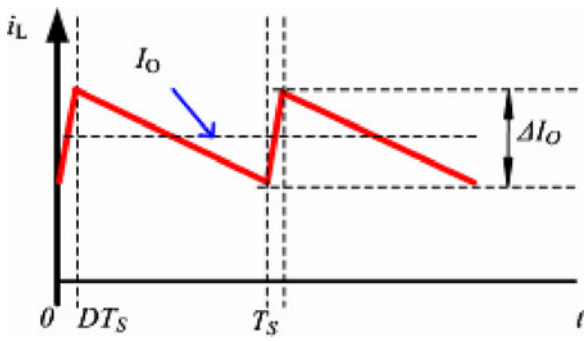

Fig. 15. Total loss versus CS inductor.

$V_{\mathrm{SPE\_SR}}$

$$P_{\mathrm{SW(ON)\_SR}} = \ln \frac{V_{C\_\mathrm{SR}} - V_{\mathrm{TH\_SR}}}{V_{C\_\mathrm{SR}} - V_{\mathrm{TH\_SR}} - I_O/g_{\mathrm{FS\_SR}}} \times (R_{\mathrm{DR\_SR}} + R_{\mathrm{G\_SR}}) \times C_{\mathrm{ISS\_SR}} \times V_{F\_\mathrm{SR}} + \ln \frac{V_{C\_\mathrm{SR}} - V_{\mathrm{TH\_SR}} - I_O/g_{\mathrm{FS\_SR}}}{V_{C\_\mathrm{SR}} - 0.9 \times V_{\mathrm{SPE\_SR}}} \times \frac{V_{F\_\mathrm{SR}} + I_O \times 1.1 \times R_{\mathrm{DR\_SR}}}{2} \times I_O \times F_S. \quad (38)$$

$$P_{\mathrm{SW(OFF)\_SR}} = \ln \frac{V_{\mathrm{TH\_SR}} + I_O/g_{\mathrm{FS\_SR}}}{V_{\mathrm{TH\_SR}}} \times (R_{\mathrm{DR(ON)\_SR}} + R_{\mathrm{G\_SR}}) \times C_{\mathrm{ISS\_SR}} \times V_{F\_\mathrm{SR}} + \ln \frac{0.9 \times V_{\mathrm{SPE\_SR}}}{V_{\mathrm{TH\_SR}} + I_O/g_{\mathrm{FS\_SR}}} \times \frac{V_{F\_\mathrm{SR}} + I_O \times 1.1 \times R_{\mathrm{DR(ON)\_SR}}}{2} \times I_O \times F_S. \quad (39)$$

c) Comparison between the calculated and simulated switching loss: The new model proposed in this paper is mainly the switching loss model for control FET that is driven by CSD. In order to verify the switching loss model, simulation for the switching loss model for control FET is conducted by using pspice model with Ltspice from Linear Technology [37]. The comparison between the calculated and simulated switching loss for control FET is shown in Fig. 16. It is observed that the calculated loss model is very close to the simulation results using pspice model.

d) Comparison between the calculated total loss and experimentally measured loss: In order to validate the accuracy of the proposed switching loss model, the calculated total loss of the synchronous buck converter as a function of load current is compared with the experimentally measured loss in Fig. 17. The parameters for the modeling are extracted from the components used in experimental prototype in Fig. 9. It is observed that the calculated loss by the loss model proposed in this paper matches the actual loss of the synchronous buck converter very well. The difference between the calculated loss and experimentally measured loss is less than 10% across all load levels from 5 to 30 A.

2) Loss Breakdown of the Synchronous Buck Converter: The loss breakdown of the calculated loss of the synchronous buck converter is illustrated in Fig. 18. It is observed that for control

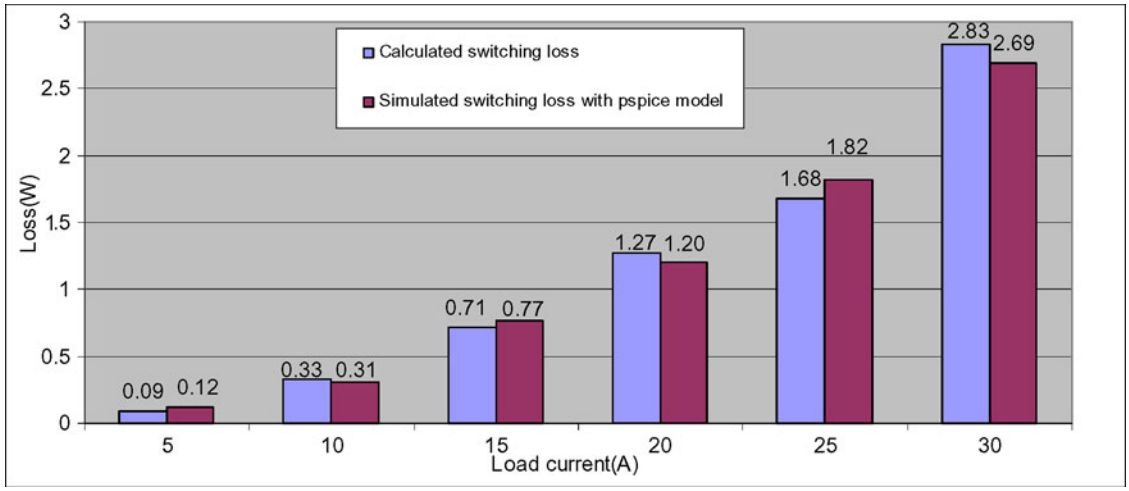

Fig. 16. Comparison between calculated switching and simulated switching loss for control FET.

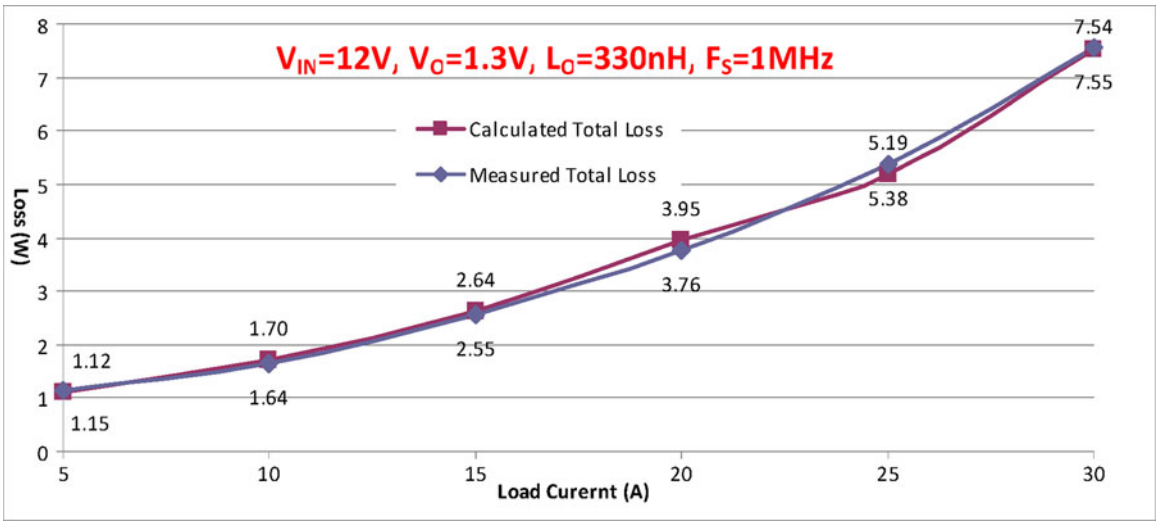

Fig. 17. Comparison between measured loss and calculated loss.

FET of the synchronous buck converter, switching loss is the dominant loss, taking up 2.83 W out of the 7.54 W of total loss (37%); while for sync FET, the conduction loss is the dominant loss that is taking up 20% of the total loss.

3) Switching Loss of Control FET Versus Load Current: The calculated switching loss of the control FET is plotted as a function of the load current in Fig. 19 to study their relationship. First-order linear fitting and second-order linear fitting are made, respectively, to the points obtained from the proposed switching loss model [38]. It is observed that the coefficient of determination R^2 for second-order polynomial fitting is 0.99 that is larger than the R^2 for first-order polynomial fitting (0.83). Since the larger R^2 is, the better the fitting represents the data, so it is inferred that second-order linear fitting matches the calculated switching loss points for control FET better. In other words, the switching loss for control FET almost increases proportionally to I_O^2.

The physics behind the quadratic relationship between the switching loss of control FET and load current is the gate-to-source voltage clamping due to the gate current diversion during drain current rising and drain current drop intervals, as analyzed in Section II. The equivalent switching circuits in these two intervals are shown in Fig. 20.

The KVL equation for drain current rising is given in (40), while the equation for drain current drops is given in (41), where T_R is the current rising time, T_F is the current falling time, and $V_{\rm ON}$ and $V_{\rm OFF}$ are the clamped gate-to-source voltages due to the gate current diversion during drain current rises or drops

$$L_S \frac{d}{dt}(i_{\rm DS}) \simeq L_S \frac{\Delta i_{\rm DS}}{\Delta t} = L_S \frac{I_O}{T_R} \simeq V_{\rm ON} - i_G R_G - V_{\rm CGS} \tag{40}$$

$$L_S \frac{d}{dt}(i_{\rm DS}) \simeq L_S \frac{\Delta i_{\rm DS}}{\Delta t} = L_S \frac{I_O}{T_F} \simeq -i_G R_G + V_{\rm CGS} - V_{\rm OFF}. \tag{41}$$

It is inferred, from (40) and (41), that both T_R and T_F are proportional to load current I_O. Therefore, the switching loss of

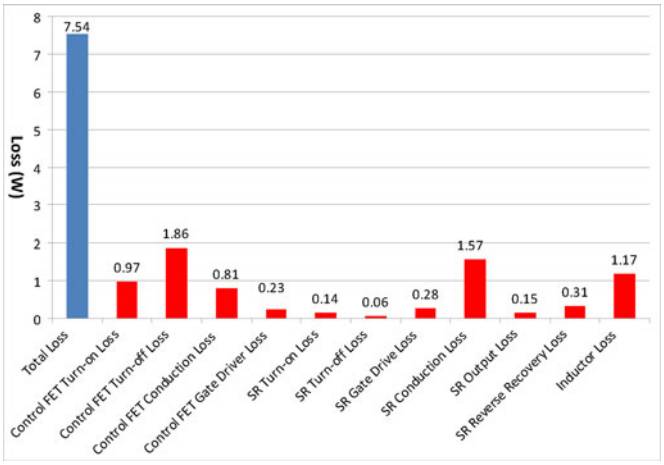

Fig. 18. Calculated loss breakdown of the synchronous buck converter.

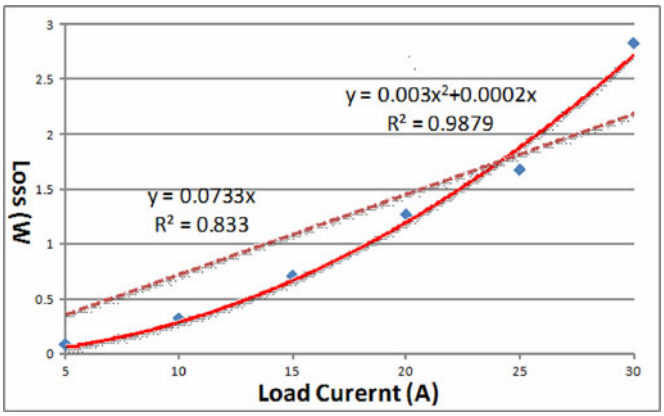

Fig. 19. Polynomial fittings of the switching loss for control FET.

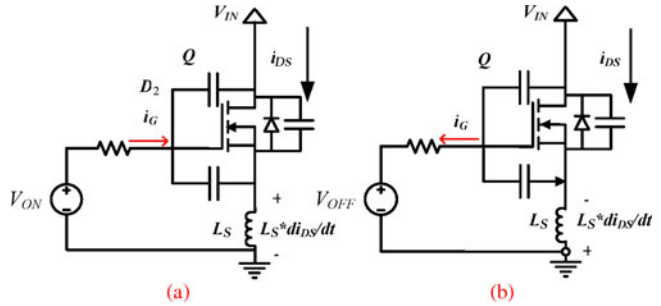

Fig. 20. Equivalent switching circuits when drain current rises and drops.

control FET, P_{SW} as approximated in (42), is almost proportional to I_O^2

$$\begin{aligned} P_{\mathrm{SW}} &= P_{\mathrm{SW\_ON}} + P_{\mathrm{SW\_OFF}} \\ &\simeq \frac{V_{\mathrm{DS\_RISING}} \times I_O \times T_R}{2} + \frac{V_{\mathrm{DS\_DROP}} \times I_O \times T_F}{2} \\ &\simeq \frac{1}{2} \times \left(\frac{V_{\mathrm{DS\_RISING}} \times L_S}{V_{\mathrm{ON}} - i_G R_G - V_{\mathrm{CGS}}} \right. \\ &\qquad \left. + \frac{V_{\mathrm{DS\_DROP}} \times L_S}{-i_G R_G + V_{\mathrm{CGS}} - V_{\mathrm{OFF}}} \right) I_O^2. \end{aligned} \tag{42}$$

4) Comparison of the Calculated Loss Among Proposed CSD, Existing CSD, and VSD: It is observed from (42) that during drain current drop interval, the clamped gate-to-source voltage V_{OFF} affects the turn-off loss to a great extent. The more negative V_{OFF} is, the smaller the turn-off loss is introduced. The V_{OFF} for proposed CSD in Fig. 1 is -3.5 V and V_{OFF} for existing CSD in [21] is -0.7 V, while for conventional VSD, V_{OFF} is roughly $+0.5$ V. Therefore, the proposed CSD in Fig. 1 is supposed to have smaller switching loss than existing CSD in [21]; both CSDs introduce smaller switching loss than conventional VSD. The calculated loss comparison among the proposed CSD in Fig. 1, existing CSD in [21], and conventional VSD is shown in Fig. 21. It is verified that the proposed CSD in Fig. 1 has the smallest total loss due to the negative gate-to-source voltage during turn-off transition. Therefore, although CSD has higher cost than the VSD, the significant performance improvement makes it a good choice for high-end applications such as servers where the performance has been limited by the figure of merits of the current semiconductor technology.

C. Verification of the Optimal Design of the CSD Inductor

To validate the optimal design of the CSD inductor, an apple-to-apple comparison between the synchronous buck converters with a 25- and 43-nH CSD inductor is made. Fig. 22 illustrates the efficiency comparison for two prototypes at 1.3 V/1 MHz output. It is noted that by comparing the CSD with 43 nH, the CSD with the optimal CSD inductor increases the efficiency at all load currents, improving from 86.1% to 87.6% by 1.5% at 20 A load and from 82.4% to 84.0% by 1.6% at 30 A load.

D. Comparison Between CSD and Commercial Products

The integrated driver-MOSFET (DrMOS) provides the optimal solution for multiphase synchronous buck converter for its high power density and reduced design time. As compared with commercially available DrMOS solutions, the synchronous buck converter driven with the optimized proposed CSD can achieve better performance.

Fig. 23 illustrates the loss comparison between optimized CSD and DrMOS from Renesas [39]. It is noted that optimized CSD has smaller loss across all load levels (5–30 A load) and at 30 A/1.3 V load in 500 kHz switching frequency, and the optimized CSD can save nearly half-watt loss (0.46 W). In addition, from the standpoint of the thermal performance, the optimized CSD is better than DrMOS since the dimension of typical DrMOS is 8 mm × 8 mm × 0.95 mm—in such a small package, even for the same amount of loss, the DrMOS has higher temperature than the optimized CSD.

While the loss comparison between optimized CSD and DrMOS-IP2005 [40] from International Rectifier is shown in Fig. 24, from which it is observed that optimized CSD can save nearly a quarter watt (0.24 W) at 1.3 V/30 A load and 1 MHz switching frequency.

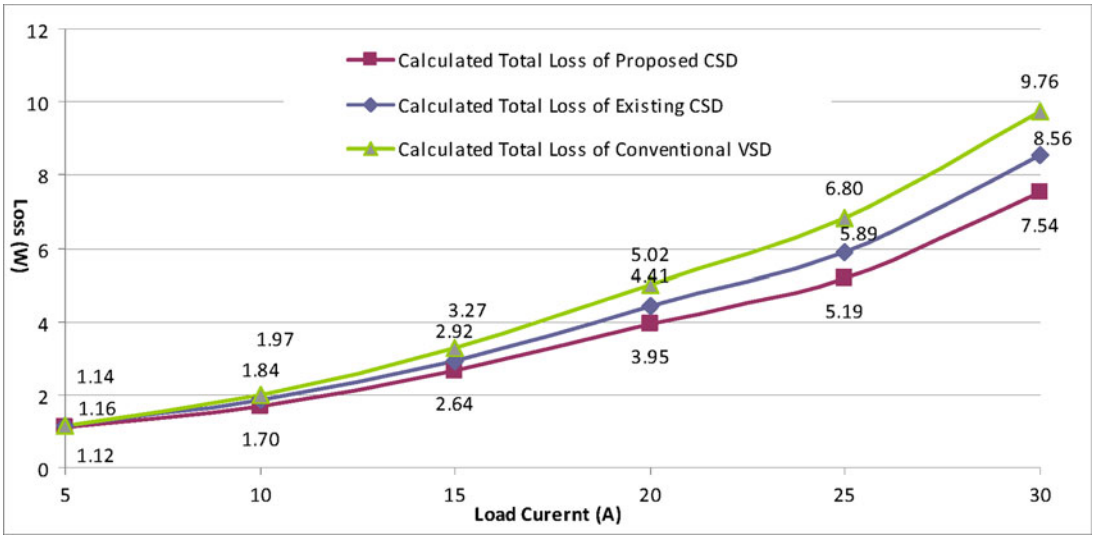

Fig. 21. Calculated loss comparison between proposed CSD (see Fig. 1), existing CSD [21], and VSD.

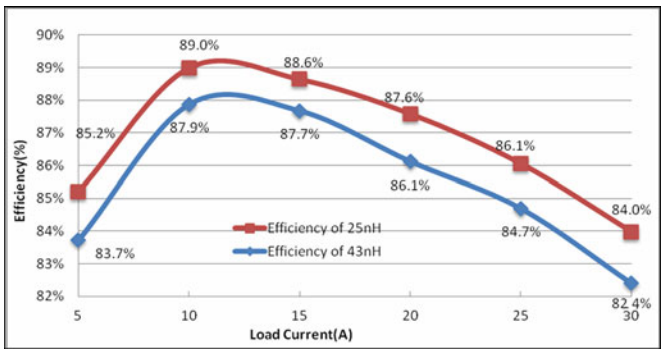

Fig. 22. Measured efficiency comparison for different CSD inductors at 12 V input, 1.3 V output, and 1 MHz.

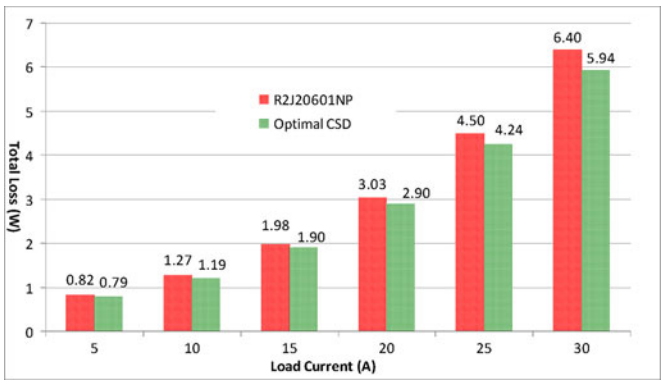

Fig. 23. Comparison between optimized CSD and DrMOS from Renesas.

V. Conclusion

In this paper, a new accurate switching loss model considering the current diversion is presented for the power MOSFET driven by a CSD, and the analytical equations for each interval to predict the switching loss are derived. Based on the proposed model, the optimal CS inductor is obtained to achieve the maximum overall efficiency of the synchronous buck converter. The experimental results verify the proposed switching loss model. The variation between the calculated loss and the experimentally measured loss is within 0.2 W from 5 to 30 A load. The modeling shows that switching loss of the control FET is nearly proportional to the square of load current because of the impact of the common source inductance and the voltage clamping due to the body diode conduction. The optimal design of the CSD inductor is also validated by the experimental results. As compared with the previous study, the CSD with the optimal inductor improves the efficiency by 1.6% at 1.3 V output 30 A load in 1 MHz switching frequency. The buck converter with the optimized CSD shows better performance than DrMOSs from Renesas and International Rectifier.

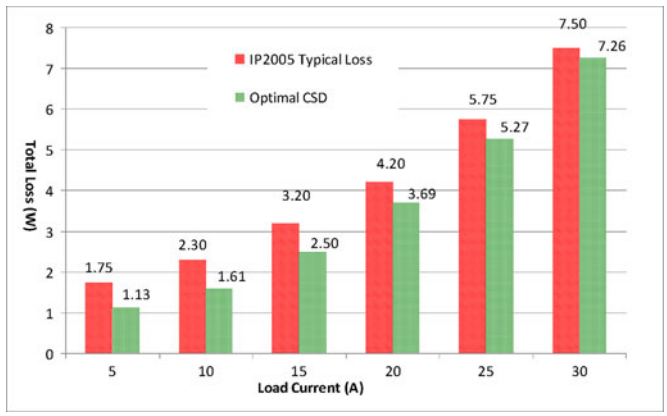

Fig. 24. Comparison between optimized CSD and DrMOS from IR.

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